AT91EB63 Evaluation Board

User Guide

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Section 1
Overview

1.1 Scope

The AT91EB63 Evaluation Board enables real-time code development and evaluation. It supports the AT91M63200 and AT91M43300.

This user guide focuses on the AT91EB63 Evaluation Board as an evaluation and demonstration platform:

- Section 1 provides an overview.
- Section 2 describes how to set up the evaluation board.
- Section 3 details the on-board software.
- Section 4 contains a description of the circuit board.
- Appendices A and B cover configuration straps and schematics, including pin connectors.

1.2 Deliverables

The evaluation board is delivered with a DB9 plug-to-DB9 socket, straight-through serial cable to connect the target evaluation board to a PC. A bare power lead with a 2.1 mm jack on one end for connection to a bench power supply is also delivered.

The evaluation board is also delivered with a CD-ROM that contains evaluation versions of software development tool kits, and the documentation that outlines the AT91 microcontroller family.

The evaluation board is capable of supporting different kinds of debugging systems, using an ICE interface or the on-board Angel™ Debug Monitor. Refer to the AT91EB63 Getting Started Tutorial documents for recommendations on using the evaluation board in a full debugging environment.

1.3 The AT91EB63 Evaluation Board

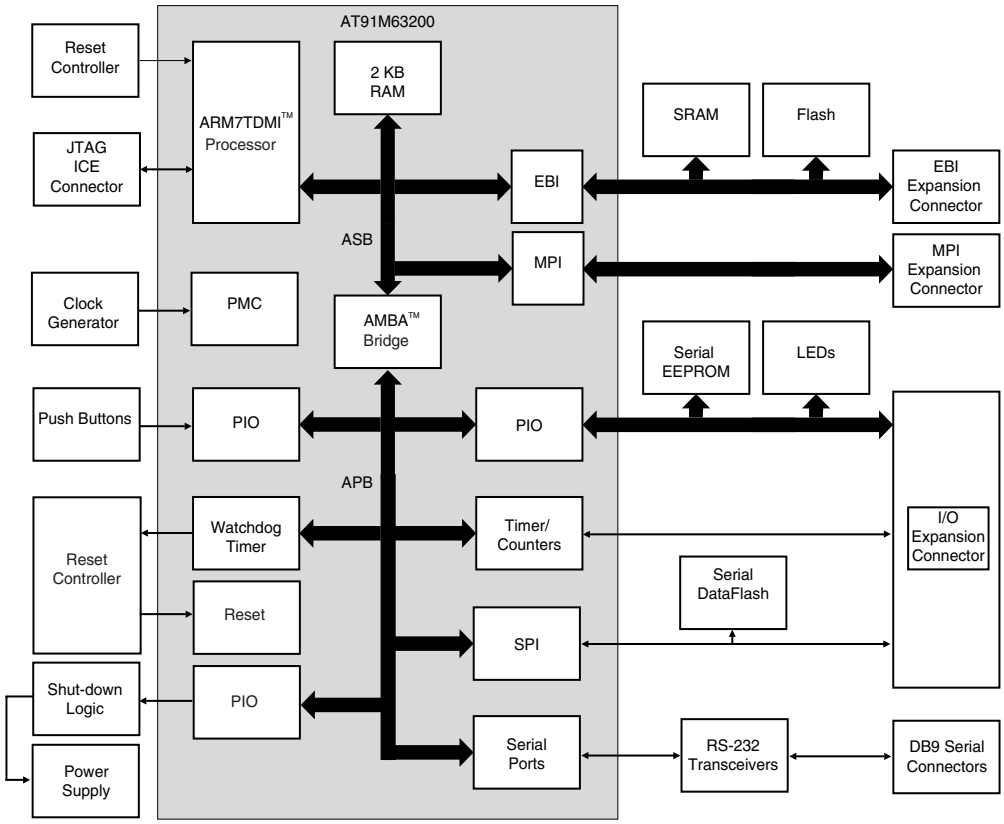
The board consists of an AT91M63200, together with several peripherals:

- Two serial ports
- Reset push button
- Four user-defined push buttons
- Eight LEDs
- 256K bytes of 16-bit SRAM (upgradable to 1 MB, see “Increasing Memory Size” on page 5-3)
- 2M bytes of 16-bit Flash (of which 1MB is available for user software)
- 2M bytes of Serial DataFlash®
- 64K bytes of Serial EEPROM
- 2 x 32-pin EBI expansion connector

- 2 x 32-pin MPI expansion connector that supports a direct connection to the EBI expansion connector
- 2 x 32-pin I/O expansion connector
- 20-pin JTAG interface connector

If required, user-defined peripherals can also be added to the board. See Appendix A for details.

Figure 1-1. AT91EB63 Evaluation Board Block Diagram



Note: The AT91EB63 Evaluation Board can also be used to evaluate the AT91M43300, as it is similar to the AT91M63200 without the MPI feature. When used with an AT91M43300, the MPI expansion connector on the AT91EB63 is not used.

Section 2

Setting Up the AT91EB63 Evaluation Board

2.1 Electrostatic Warning

The AT91EB63 Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic conditions. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

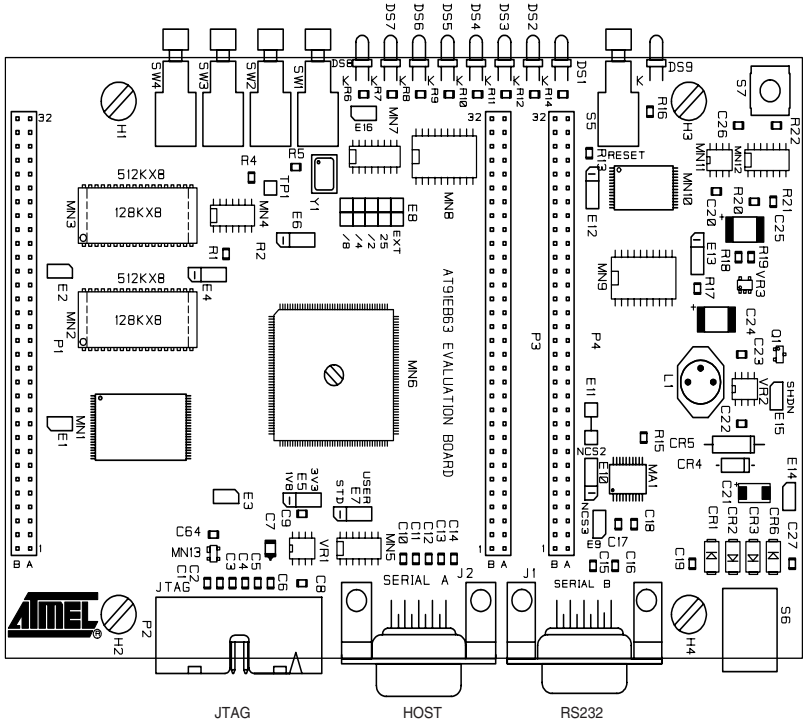
Requirements in order to set up the AT91EB63 Evaluation Board are:

- The AT91EB63 Evaluation Board
- The DC power supply capable of supplying 7.5V to 14V at 1A (not supplied)

2.3 Layout

Figure 2-1 shows the layout of the AT91EB63 Evaluation Board.

Figure 2-1. Layout of the AT91EB63 Evaluation Board



2.4 Jumper Settings

E8 is used to select the clock frequency. The origin of the clock frequency is a 25 MHz on-board oscillator (default) or external source via the EBI extension connector.

E7 is used to boot on standard or user programs. For standard operations, set it in the STD position.

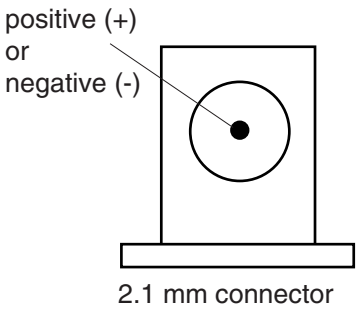
E5 is used to select the core power supply of the AT91M63200. For operation at 25 MHz, set it in the 3V3 position.

For more information about jumpers and other straps, see Appendix A.

2.5 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (S6) shown below. The polarity of the power supply is not critical. The minimum voltage required is 7V.

Figure 2-2. DC Power Supply



The board has a voltage regulator providing +3.3V. The regulator allows the input voltage to be from 7V to 12V. When you switch the power on, the red LED marked POWER lights up. If it does not, switch off and check the power supply connections.

2.6 Measuring Current Consumption on the AT91M63200

The board is designed to generate the power for the AT91 product, and only the AT91 product, through the wire link E11. This feature enables measurements to be made of the current consumption of the AT91 product.

The AT91M63200 has its own power pins and its consumption can be measured through the wire link E5. See Appendix A for further details.

2.7 Testing the AT91EB63 Evaluation Board

In order to test the AT91EB63 evaluation board, the following procedure must be followed:

1. Hold down the SW1 button and power up the board, or generate a reset and wait for the light sequence on each LED to complete. All the LEDs light once and the DS1 LED remains lit.
2. Release the SW1 button. The LEDs DS1 to DS7 light up one after the other. If any of the LEDs lights up twice, there is a fault.

The LEDs represent the following components:

- DS1 for the internal RAM
- DS2 for the external RAM
- DS3 for the MPI internal test
- DS4 for the external Flash
- DS5 for the DataFlash
- DS6 for the EEPROM
- DS7 for the USART
- DS8 is reserved

If a test is not carried out, the corresponding LED remains unlit and the test sequence restarts.

Section 3

The On-board Software

3.1 AT91EB63 Evaluation Board

The AT91EB63 Evaluation Board embeds an AT49BV1604 Flash device programmed with default software. Only the lowest 8 x 8K byte sectors are used. The remaining sectors are user-definable, and can be programmed using one of the Flash downloader solutions offered in the AT91 library.

When delivered, the Flash device contains:

- The Boot Program
- The Functional Test Software
- The SRAM Downloader
- The Angel Debug Monitor
- A Default User Boot with a Default Application

The boot, FTS and SRAM downloader are in sector 0 of the Flash. This sector is locked to prevent accidental erase, but it can be unlocked by applying 12V to the RESET pin.

3.2 The Boot Program

The boot program configures the AT91M63200, and thus controls the memory and other board components.

The boot program is started at reset if E7 is in the STD position. If E7 is in the USER position, the AT91M63200 boots from address 0x1100000 in the Flash, which must have a user-defined boot.

The boot program first initializes the EBI, then executes the REMAP procedure and checks the state of the buttons.

- When the button SW1 is pressed:

  All the LEDs light together

  The DS1 LED remains lit until SW1 is released

  The Functional Test Software (FTS) is started

- When the button SW2 is pressed:

  All the LEDs light together

  The DS2 LED remains lit until SW2 is released

  The SRAM downloader is activated

- When SW3 or SW4 is pressed or no buttons are pressed:

  Branch at address 0x0100 4000

  The Angel Debug Monitor starts from this address by recopying itself in external SRAM

3.3 Programmed Default Memory Mapping

The following table defines the mapping defined by the boot program.

Table 1. Memory Map

Part Name	Start Address	End Address	Size	Device
MN1	0x1000000	0x011FFFFF	2M Bytes	Flash AT91BV1604
MN2-MN3	0x02000000	0x02040000	256K Bytes	SRAM

The boot program, FTS and SRAM Downloader are in sectors 1 and 2 of the Flash device. Sectors 3 to 8 support the Angel Debug Monitor.

Sector 24 at address 0x0110 0000 must be programmed with a boot sequence to be debugged. This sector can be mapped at address 0x0100 0000 (or 0x0 after a reset) when the switch E7 is in the USER position.

3.4 The SRAM Downloader

The SRAM downloader allows an application to be loaded in the SRAM at the address 0x02000000, and then activates it. It is started by the boot if the SW2 button is pressed at reset.

The procedure is as follows:

1. Connect the AT91EB63 Evaluation Board to the host PC serial A connection using the straight serial cable provided.
2. Power on or press RESET, holding down the SW2 button at the same time. Wait for DS2 to light up and then release SW2.
3. Start the BINCOM utility, available in the AT91 Library, on the host computer:

   Select the port for communications (COM1 or COM2, depending on where you connected the serial cable on the host PC) and the baud rate for communications (115200 bds, 1 stop, no parity).

   Open the file to be downloaded and send it. Wait for the end of the transfer.
4. Press any button to end the download. The control is switched to the address 0x02000000.

3.5 The Angel Monitor

The Angel monitor is located in the Flash from 0x01002000 up to 0x0100FFFF. The boot program starts it if no button is pressed at reset.

When the Angel starts, it recopies itself in SRAM, thus allowing it to run faster. The SRAM used by the Angel is from 0x2020000 to 0x2040000, for example, the highest half of the SRAM.

The Angel on the AT91EB63 Evaluation Board can be upgraded regardless of the version programmed on it.

Note that if the debugger is started through ICE while the Angel monitor is on, the Advanced Interrupt Controller (AIC) and the USART channels are configured and running.

Section 4

Circuit Description

4.1 AT91M63200 Processor

Figure 6-1 in “Appendix B – Schematics” shows the AT91M63200. The footprint is for a 176-pin TQFP package.

Strap E6 enables the user to choose between the standard ICE debug mode and the JTAG boundary scan mode of operation.

The operating mode is defined by the state of the JTAGSEL input detected at reset.

Wirelink E11 (see Figure 6-3 in “Appendix B – Schematics”) can be removed by the user to allow measurement of the current consumed by the whole microcontroller (V_{DDIO} and V_{DDCORE}).

4.2 Expansion Connectors and JTAG Interface

The three expansion connectors – I/O expansion connector, MPI expansion connector, EBI expansion connector – and the JTAG interface are described below.

4.2.1 I/O Expansion Connector

The I/O expansion connector makes the general-purpose I/O (GPIO) lines, VCC3V3 and Ground available to the user. Configuration straps E4, E9, E12, E13, E15 and E16 are used to select between the I/O lines being used by the evaluation board or by the user via the I/O expansion connector. The connector is not fitted at the factory; however, the user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch.

4.2.2 EBI Expansion Connector

The schematic (Figure 6-6 in “Appendix B – Schematics”) also shows the EBI expansion connector, which, like the I/O expansion connector, is not fitted at the factory. The user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch to gain access to the data, address, chip select, read/write, oscillator output and external wait request pins. Pin B4 on this connector can be used to apply an external clock frequency to the board, assuming the clock select jumper is fitted accordingly (see Appendix A). VCC3V3 and Ground are also available on this connector. When the E2 configuration strap is open, the user can connect the EBI expansion connector to the MPI expansion connector of another AT91EB63 Evaluation Board without fearing any conflict problem.

4.2.3 MPI Expansion Connector

The MPI expansion connector and EBI expansion connector pinouts are compatible, so the user can connect the EBI expansion connector of another AT91 Evaluation Board to this MPI expansion connector and dialog with it via the MPI feature. Connection strap E10 enables the MPI to be accessed via the NCS2 or the NCS3 select signals of this other board. This connector is not fitted at the factory, but the user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch.

4.2.4 JTAG Interface

An ARM-standard 20-pin box header (P2) is provided to enable connection of an ICE interface to the JTAG inputs on the AT91. This allows code to be developed on the board without using system resources such as memory and serial ports.

4.3 Memories

The schematic (Figure 6-2 in “Appendix B – Schematics”) shows one AT49BV1604 2-Mbyte, 16-bit Flash, one AT45DB161 2-Mbyte serial DataFlash, one AT24C512 64-Kbyte EEPROM and two 128K/512K x 8 SRAM devices.

Note: The AT91EB63 is fitted with two 128K x 8 SRAM devices.

Strap E7 shown on this schematic is used to select the part of the1-Mbyte Flash that is to be accessed. This is to enable users to Flash download a user-defined application into the second part of the Flash and to boot from it.

4.4 Power, Crystal Oscillator and Clock Distribution

The system clock is derived from a single 25 MHz crystal oscillator. This is divided by a 4-bit binary counter to give alternate clock frequencies of 25 MHz divided by 2, 4 or 8. The system clock frequency is selected by fitting a jumper link in one position of the link field (E8) and details of this can be found in Appendix A. One position in E8 selects an external oscillator to be applied via the expansion bus interface.

Note: The 4-bit binary counter is not fitted at the factory (this function is optional).

The voltage regulator provides 3.3V to the board and lights the red POWER LED (DS9) when operating. Power can be applied via the 2.1 mm connector to the regulator in either polarity because of the diode-rectifying circuit. Another regulator allows the user to power the AT91M63200 core 1.8V from the 3.3V voltage using the E5 strap.

When closed, the E15 strap allows the user to shut down the 3.3V regulator by simply clearing the PA22 microcontroller PIO. A 100 µF capacitor powers this feature while shut down. The board can be reactivated by pushing the S7 SMT push button.

4.5 Push Buttons, LEDs, Reset and Serial Interfaces

The IRQ0, PB3, PB4 and PB5 switches are debounced and buffered.

A supervisory circuit has been included in the design to detect and, consequently, reset the board when the 3.3V supply voltage drops below 3.08V. Note that this voltage can be changed, depending on the board production series. The supervisory circuit also provides a debounced reset signal. This device can also generate the reset signal in case of watchdog timeout as the pin NWDOVF of the AT91M63200 is connected on its input $\overline{\text{MR}}$.

Another supervisory circuit initializes separately the microcontroller embedded JTAG/ICE interface when the 3.3V supply voltage drops below 3.08V. Note that this voltage can be changed, depending on the board production series. These separated reset lines allow the user to reset the board without resetting the JTAG/ICE interface while debugging.

The schematic (Figure 6-4 in “Appendix B – Schematics”) also shows eight general-purpose LEDs connected to Port B PIO pins (PB8 to PB15).

Two 9-way D-type connectors (J1/2) are provided for serial port connection.

Serial Port A (J2) is used primarily for host PC communication and is a DB9 female connector. TXD and RXD are swapped so that a straight-through cable can be used. CTS and RTS are connected together, as are DCD, DSR and DTR.

Serial Port B (J1) is a DB9 male connector with TXD and RXD obeying the standard RS-232 pinout. Apart from TXD, RXD and Ground, the other pins are not connected.

A MAX3223 device (MA1) and associated bulk storage capacitors provide RS-232 level conversion.

4.6 Layout Drawing

The layout diagram (Figure 6-1 in “Appendix B – Schematics”) shows an approximate floorplan for the board. This has been designed to give the smallest board area, while still providing access to all test points, links and switches on the board.

The board is provided with four mounting holes, one at each corner, into which feet are attached. The board has two signal layers and two power planes.

Section 5

Appendix A – Configuration Straps

5.1 Clock Selection Switch (E8)

The E8 switch is used to select the clock frequency. The frequency options are 25 MHz, 25 MHz divided by 2, 4 or 8, or an external clock applied via the EBI expansion connector.

E8

2	4	6	8	10
1	3	5	7	9
EXT	**25**	**/2**	**/4**	**/8**

Note: Prior to using this function, users must fit the 4-bit binary counter used to divide the 32.768 MHz clock.

5.2 Configuration Straps (E1 - E7, E9 - E16)

By adding the I/O, MPI and EBI expansion connectors, users can connect their own peripherals to the evaluation board. These peripherals may require more I/O lines than available while the board is in its default state. Extra I/O lines can be made available by disabling some of the on-board peripherals or features. This is done using the configuration straps detailed below. Some of these straps present a default wire (notified by the default mention) that must be cut before soldering the strap.

E1	Flash Reset
Closed(1)	The on-board reset signal is connected to the Flash NRESET input.
Open	The on-board reset signal is not connected to the Flash NRESET input.

E2	On-board A23/CS4 Signal
Closed(1)	AT91 A23/CS4 signal connected to the EBI expansion connector (P1-B21).
Open	AT91 A23/CS4 signal connected to the EBI expansion connector (P1-B21). This authorizes users to connect the EBI expansion connector of this board to the MPI expansion connector of another AT91EB63 board without conflict problems.

E3	On-board Boot Chip Select
Closed[1]	AT91 NCS0 select signal connected to the Flash memory.
Open	AT91 NCS0 select signal not connected to the Flash memory. This authorizes users to connect the corresponding select signal to their own resources via the EBI expansion connector.

E4	Push-button Enabling
Closed[1]	SW1 - 4 inputs to the AT91 are valid.
Open	SW1 - 4 inputs to the AT91 are not valid. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

E5	Core Power Supply Selection
2-3	The AT91 core is powered by a 3.3V power supply.
1-2	The AT91 core is powered by a 1.8V power supply. In this case, the maximum frequency that can be used is 25 MHz divided by 2 (position **/2** on E8).

E6	JTAGSEL
2-3[1]	AT91 standard ICE debug feature enabled.
1-2	IEEE 1149.1 JTAG boundary scan feature enabled.

E7	User or Standard Boot Selection
1-2	The first half of the Flash memory is accessible at its base address.
2-3	The second half of the Flash memory is accessible at its base address. This authorizes users to download their own application software in this part and boot on it.

E9	RS-232 Driver Enabled
Closed[1]	The RS-232 transceivers are enabled.
Open	The RS-232 transceivers are disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

E10	MPI Chip Select Selection
2-3	When connecting the MPI expansion connector of this board to the EBI expansion connector of another Atmel evaluation board, the MPI is selected by the NCS2 select signal.
1-2	When connecting the MPI expansion connector of this board to the EBI expansion connector of another Atmel evaluation board, the MPI is selected by the NCS3 select signal.

E12[2]	Serial DataFlash Enabling
Closed[1]	AT91 NPCS0 select signal is connected to the serial DataFlash memory.
Open	AT91 NPCS0 select signal is not connected to the serial DataFlash memory. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

E13	Serial EEPROM Enabling
1-2	EEPROM communication disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.
2-3[1]	EEPROM communication enabled.

E15	Shutdown Enabling
Open	Power supply shutdown feature is disabled.
Closed	Power supply shutdown feature is enabled. The user can shut down the board power supply by clearing the PA22 AT91M63200 PIO. The system can be re-activated by pushing the S7 SMT push button (the reset signal is activated).

E16	Frequency Auto-detect Enabling
Closed[1]	This enables the AT91M63200 to detect the frequency of the oscillator soldered on the board.
Open	This feature is not available. Users can connect the corresponding PIO to their own resources via the I/O expansion connector.

Notes: 1. Hardwired default position: To cancel this default configuration, cut the wire on the board.
2. E12 is a 3-pin strap, with positions 1.2 and 2.3 allowed. The default is position 1.2. This position is required to enable the pull-up R13 on NPCS0 when E12 is closed, and to disable the DataFlash from the SPI lines when E12 is open.

5.3 Power Consumption Measurement Strap (E11)

The E11 strap enables you to connect an ammeter to measure the AT91M63200 global consumption (V_{DDCORE} and V_{DDIO}). You can measure the core consumption by connecting another ammeter between E5 1-2 or 2-3, depending on the power supply you are using to power the core.

The current measured on E11 is the total current required by the AT91M63200 on both V_{DDIO} and V_{DDPLL}. It is also the current consumed by the switching regulator VR1 that provides the 1.8V supply.

5.4 Ground Links (E14)

The E14 strap enables the user to connect the electrical and mechanical grounds.

5.5 Increasing Memory Size

The AT91EB63 Evaluation Board is supplied with two 128K x 8 byte SRAM memories. If, however, the user needs more than 256K bytes of memory, the user can replace these devices with two 512K x 8, 3.3V, 10/15 ns SRAMs, giving in total 1024K bytes.

Section 6

Appendix B – Schematics

The following schematics are appended:

Figure 6-1. PCB Layout

Figure 6-2. Memories

Figure 6-3. Power, Crystal Oscillator, Clock Distribution and Power Supply Shutdown

Figure 6-4. Push Buttons, LEDs, Reset and Serial Interface

Figure 6-5. AT91M63200

Figure 6-6. I/O, MPI and EBI Expansion Connectors and JTAG Interface

The pin connectors are indicated on the schematics:

- P1 = EBI Expansion Connector (Figure 6-6)
- P2 = JTAG Interface (Figure 6-6)
- P3 = I/O Expansion Connector (Figure 6-6)
- P4 = MPI Expansion Connector (Figure 6-6)
- J1 = Serial B (Figure 6-4)
- J2 = Serial A (Figure 6-4)

Figure 6-1. PCB Layout

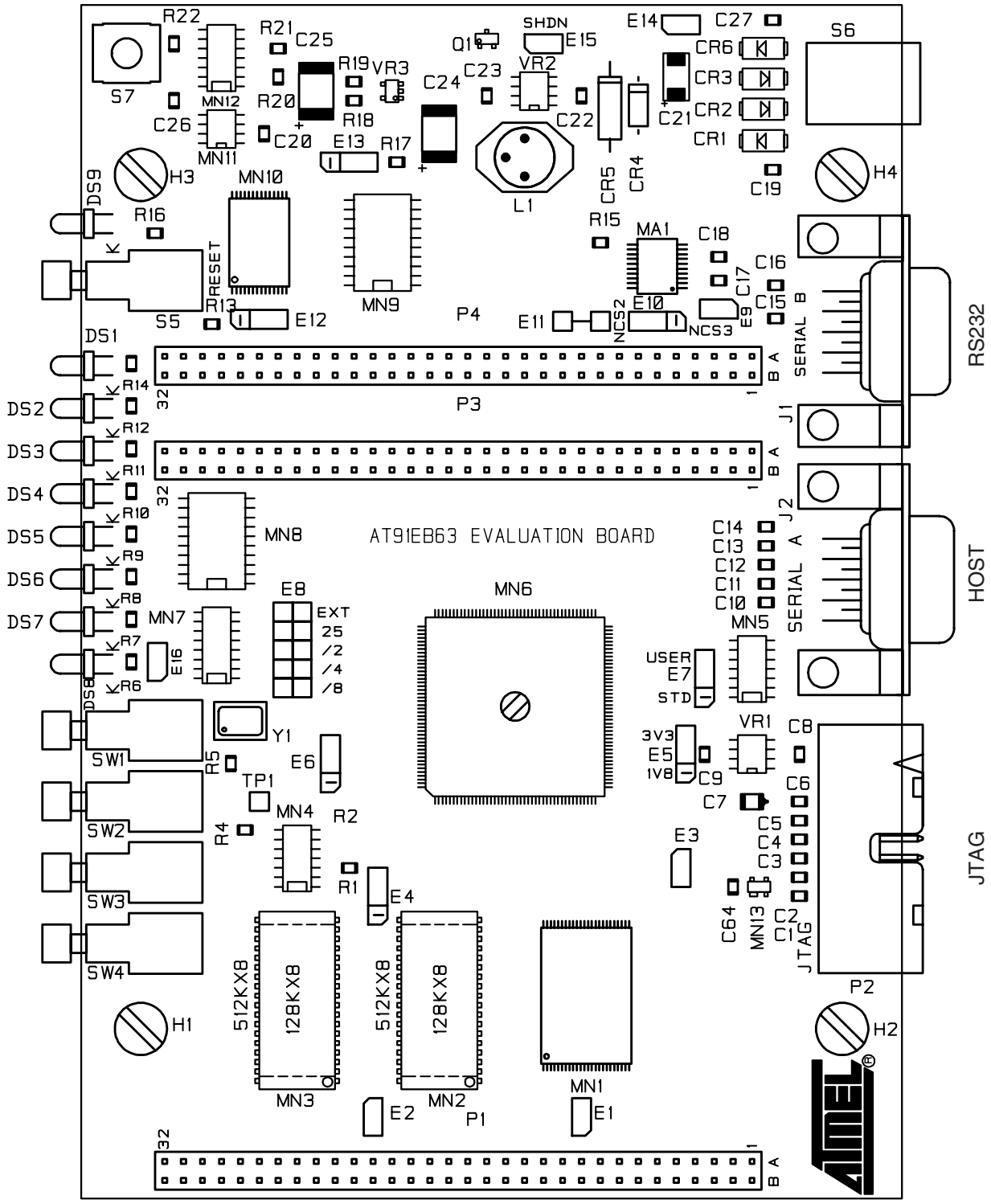
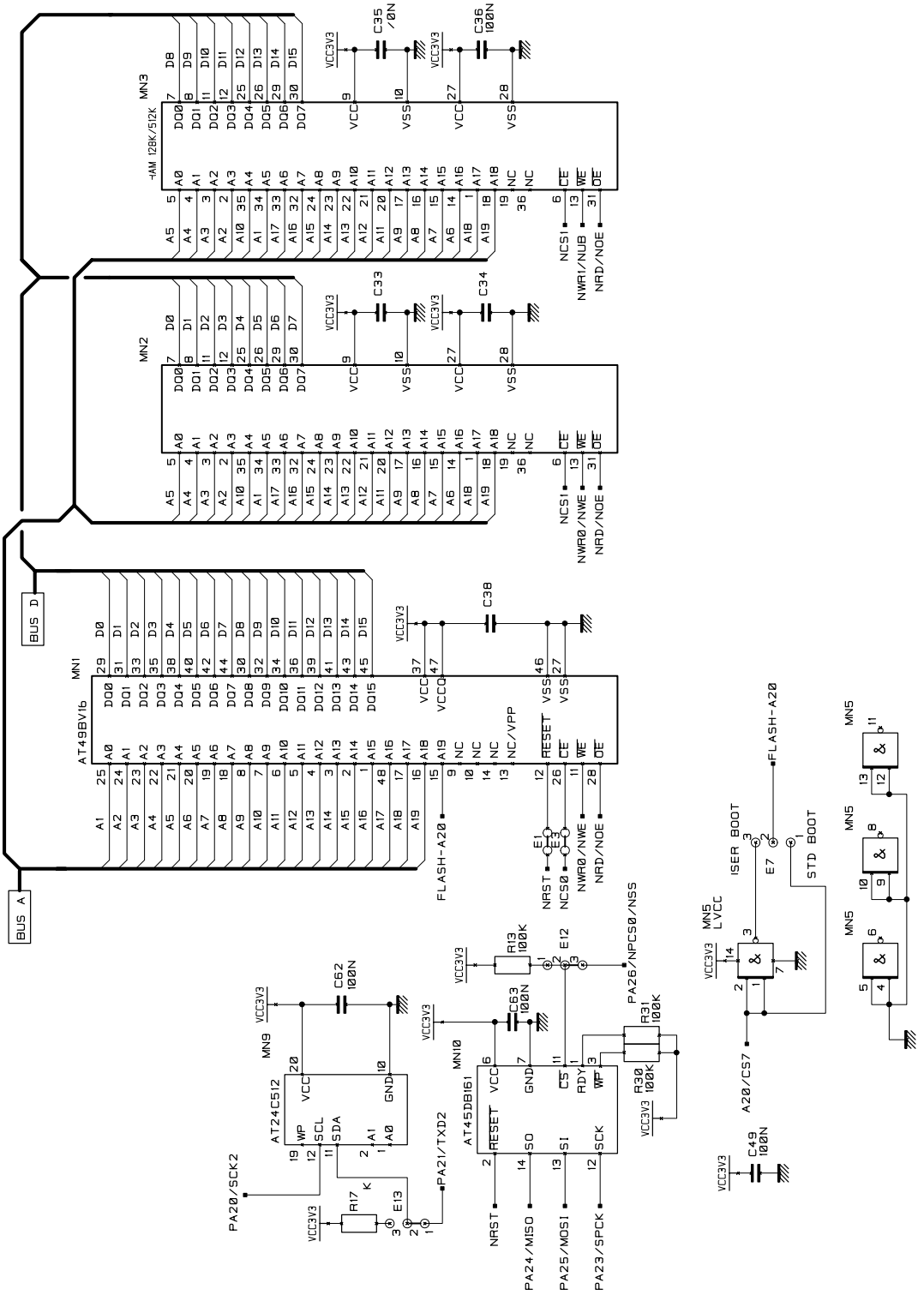


Figure 6-2. Memories



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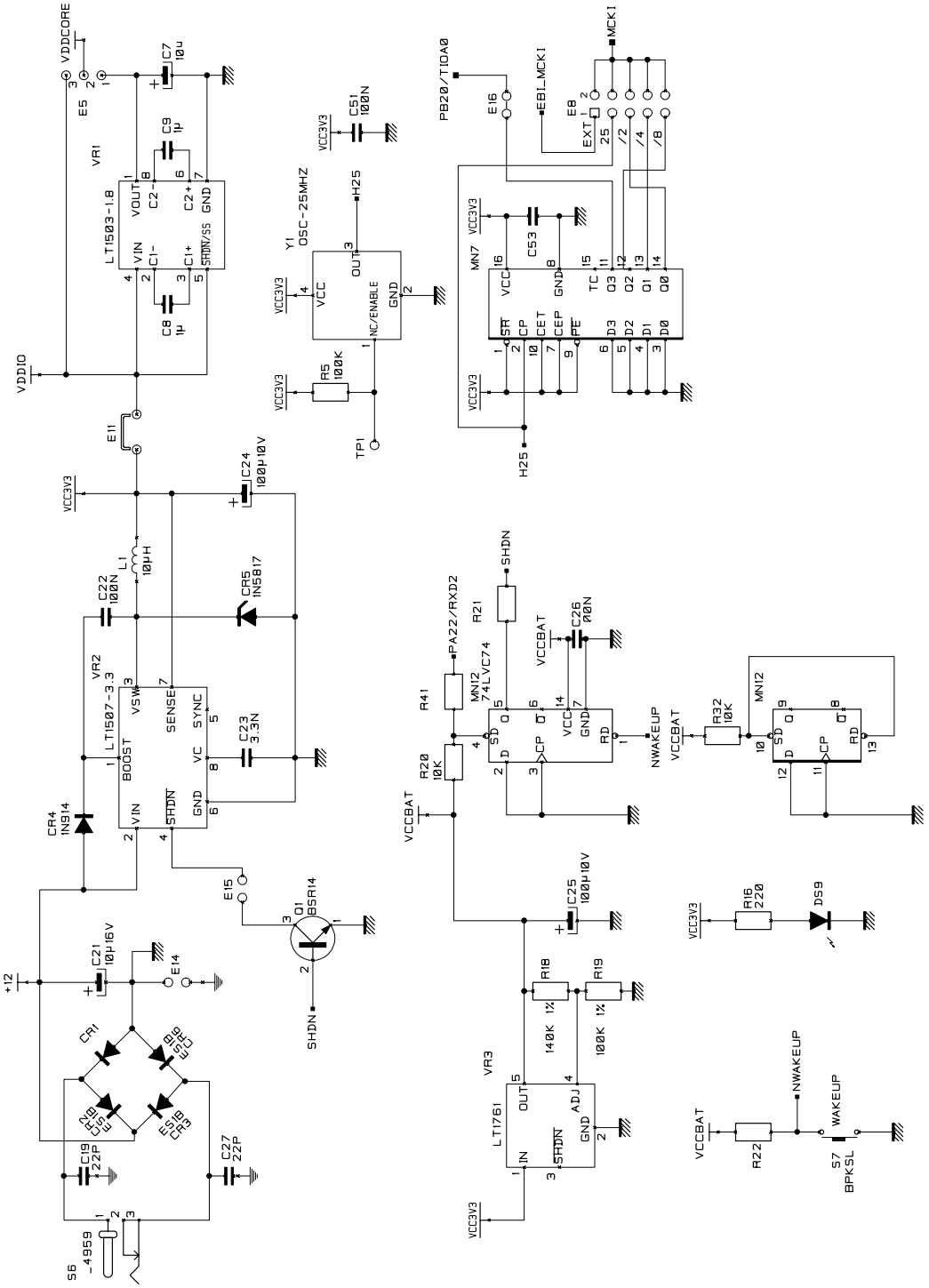


Figure 6-4. Push Buttons, LEDs, Reset and Serial Interface

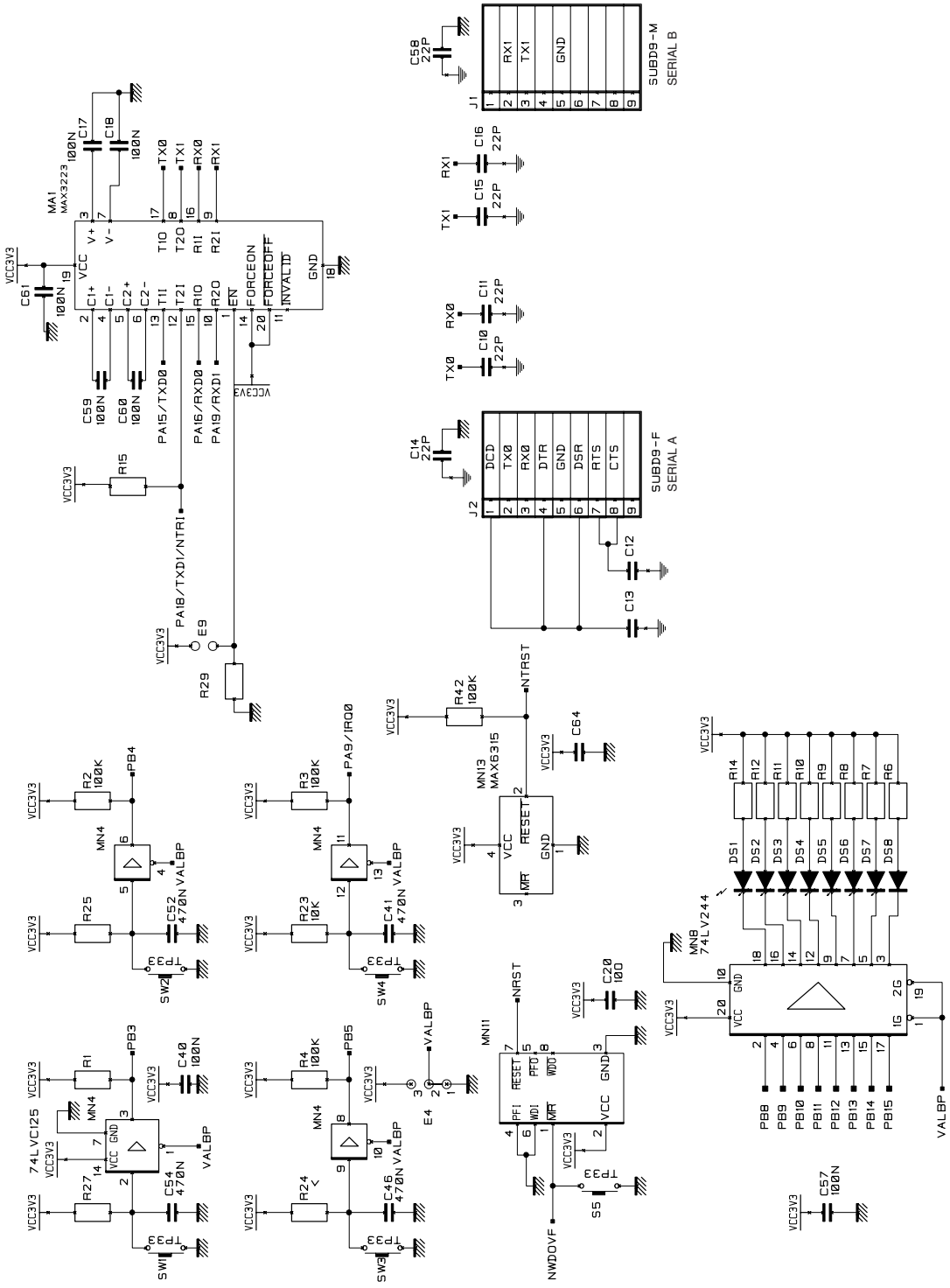


Figure 6-5. AT91M63200

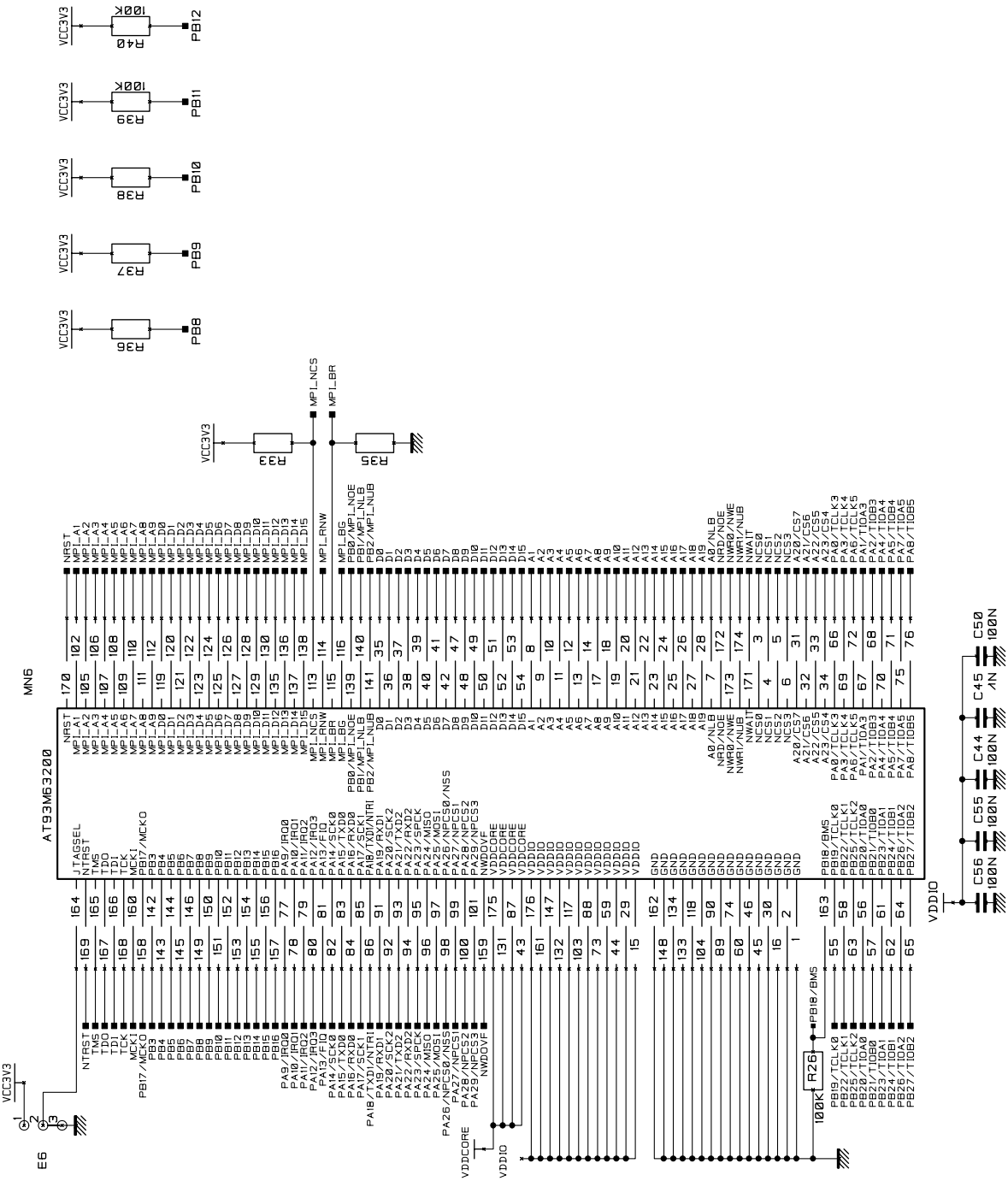
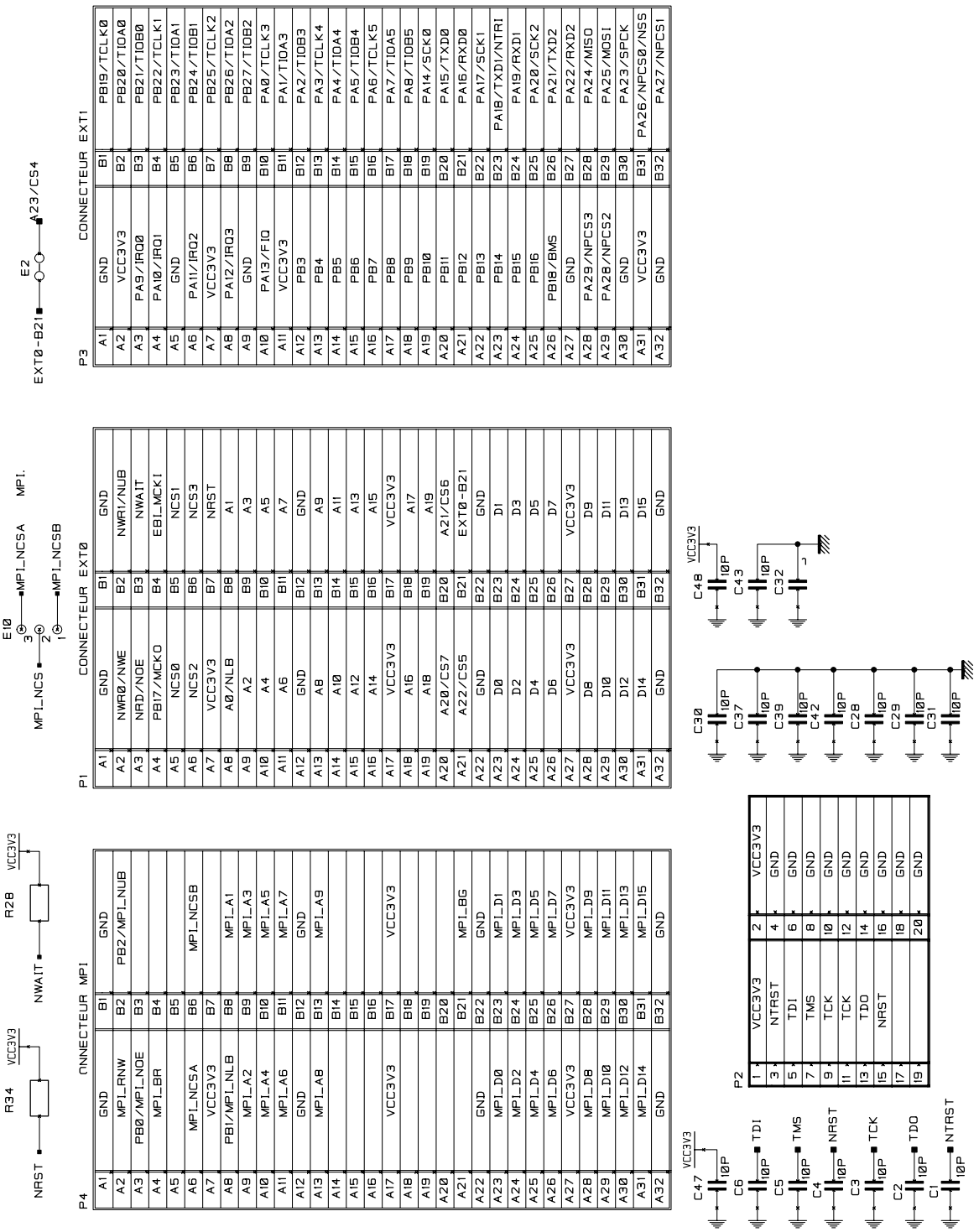


Figure 6-6. I/O, MPI and EBI Expansion Connectors and JTAG Interface



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